**CARDAMOM PLANTERS'ASSOCIATION COLLEGE**
**BODINAYAKANUR.**
**DEPARTMENT OF PHYSICS (SF)**

**UNIT- I**

Fabrication of IC Integrated circuit fabrication process: oxidation, diffusion, ion implantation, photolithography, etching, chemical vapor deposition, sputtering, twin-tub CMOS process. Sheet resistance, design of resistors.

## Semiconductor Fabrication Processes

Starting with a uniformly doped silicon wafer, the fabrication of integrated circuits (IC's) needs hundreds of sequential process steps. The most important process steps used in the semiconductor fabrication are:

## Lithography

Lithography is used to transfer a pattern from a photo mask to the surface of the wafer. For example the gate area of a MOS transistor is defined by a specific pattern. The pattern information is recorded on a layer of photoresist which is applied on the top of the wafer. The photoresist changes its physical properties when exposed to light (often ultraviolet) or another source of illumination (e.g. X-ray). The photoresist is either developed by (wet or dry) etching or by conversion to volatile compounds through the exposure itself. The pattern defined by the mask is either removed or remained after development, depending if the type of resist is positive or negative. For example the developed photoresist can act as an etching mask for the underlying layers.

## Etching

Etching is used to remove material selectively in order to create patterns. The pattern is defined by the etching mask, because the parts of the material, which should remain, are protected by the mask. The unmasked material can be removed either by wet (chemical) or dry (physical) etching. Wet etching is strongly isotropic which limits its application and the etching time can be controlled difficultly. Because of the so-called under-etch effect, wet etching is not suited to transfer patterns with sub-micron feature size. However, wet

etching has a high selectivity (the etch rate strongly depends on the material) and it does not damage the material. On the other side dry etching is highly anisotropic but less selective. But it is more capable for transferring small structures.

**Deposition**

A multitude of layers of different materials have to be deposited during the IC fabrication process. The two most important deposition methods are the physical vapor deposition (PVD) and the chemical vapor deposition (CVD). During PVD accelerated gas ions sputter particles from a sputter target in a low pressure plasma chamber. The principle of CVD is a chemical reaction of a gas mixture on the substrate surface at high temperatures. The need of high temperatures is the most restricting factor for applying CVD. This problem can be avoided with plasma enhanced chemical vapor deposition (PECVD), where the chemical reaction is enhanced with radio frequencies instead of high temperatures. An important aspect for this technique is the uniformity of the deposited material, especially the layer thickness. CVD has a better uniformity than PVD.

**Chemical Mechanical Planarization**

Processes like etching, deposition, or oxidation, which modify the topography of the wafer surface lead to a non-planar surface. Chemical mechanical planarization (CMP) is used to plane the wafer surface with the help of a chemical slurry. First, a planar surface is necessary for lithography due to a correct pattern transfer. Furthermore, CMP enables indirect pattering, because the material removal always starts on the highest areas of the wafer surface. This means that at defined lower lying regions like a trench the material can be left. Together with the deposition of non-planar layers, CMP is an effective method to build up IC structures.

**Oxidation**

Oxidation is a process which converts silicon on the wafer into silicon dioxide. The chemical reaction of silicon and oxygen already starts at room temperature but stops after a very thin native oxide film. For an effective oxidation rate the wafer must be settled to a furnace with oxygen or water vapor at elevated temperatures. Silicon dioxide layers are

used as high-quality insulators or masks for ion implantation. The ability of silicon to form high quality silicon dioxide is an important reason, why silicon is still the dominating material in IC fabrication.

**Ion Implantation**

Ion implantation is the dominant technique to introduce dopant impurities into crystalline silicon. This is performed with an electric field which accelerates the ionized atoms or molecules so that these particles penetrate into the target material until they come to rest because of interactions with the silicon atoms. Ion implantation is able to control exactly the distribution and dose of the dopants in silicon, because the penetration depth depends on the kinetic energy of the ions which is proportional to the electric field. The dopant dose can be controlled by varying the ion source. Unfortunately, after ion implantation the crystal structure is damaged which implies worse electrical properties. Another problem is that the implanted dopants are electrically inactive, because they are situated on interstitial sites. Therefore after ion implantation a thermal process step is necessary which repairs the crystal damage and activates the dopants.

**Diffusion**

Diffusion is the movement of impurity atoms in a semiconductor material at high temperatures. The driving force of diffusion is the concentration gradient. There is a wide range of diffusivities for the various dopant species, which depend on how easy the respective dopant impurity can move through the material. Diffusion is applied to anneal the crystal defects after ion implantation or to introduce dopant atoms into silicon from a chemical vapor source. In the last case the diffusion time and temperature determine the depth of dopant penetration. Diffusion is used to form the source, drain, and channel regions in a MOS transistor. But diffusion can also be an unwanted parasitic effect, because it takes place during all high temperature process steps.

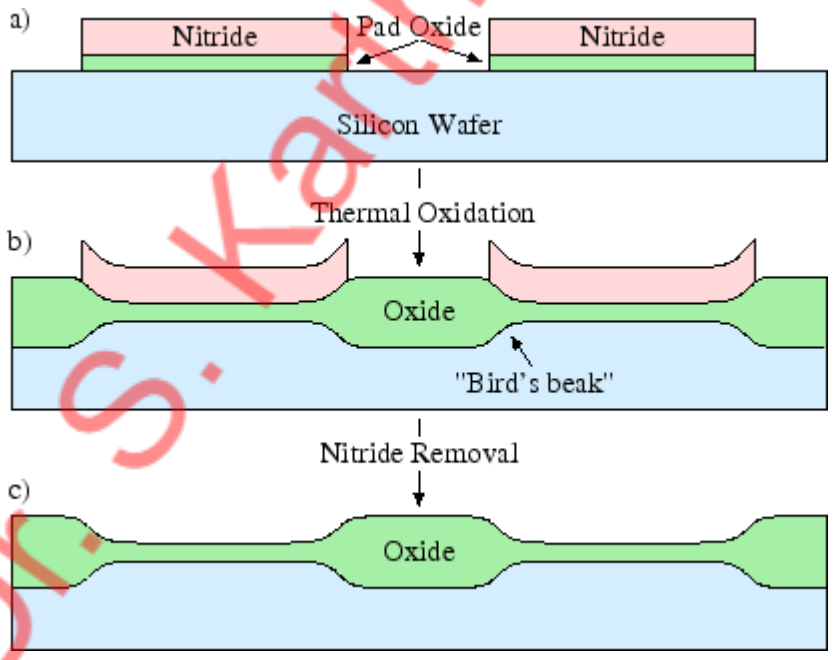
**Isolation Techniques**

Thermal grown oxide is mainly used as isolation material in semiconductor fabrication. For the isolation of neighboring MOS transistors there exist two techniques, namely Local Oxidation of Silicon and Shallow Trench Isolation. The differences in their

process flow and their final oxide shapes are described in the following.

### Local Oxidation of Silicon

**Loc**al **O**xidation **o**f **S**ilicon (LOCOS) is the traditional isolation technique. At first a very thin silicon oxide layer is grown on the wafer, the so-called pad oxide. Then a layer of silicon nitride is deposited which is used as an oxide barrier. The pattern transfer is performed by photolithography. After lithography the pattern is etched into the nitride. The result is the nitride mask as shown in Fig. 1.1a, which defines the active areas for the oxidation process. The next step is the main part of the LOCOS process, the growth of the thermal oxide. After the oxidation process is finished, the last step is the removal of the nitride layer. The main drawback of this technique is the so-called bird's beak effect and the surface area which is lost to this encroachment. The advantages of LOCOS fabrication are the simple process flow and the high oxide quality, because the whole LOCOS structure is thermally grown.




Process sequence for local oxidation of silicon (LOCOS).



### A.1 IC Fabrication Steps

The basic IC fabrication steps will be described in the following sections. Some of these steps may be carried out many times, in different combinations and/or processing

conditions during a complete fabrication run.

### A.1.1 Silicon Wafers

The starting material for modern integrated circuits is very-high-purity, single-crystal silicon. The material is initially grown as a single crystal ingot. It takes the shape of a steel-gray solid cylinder 10 cm to 30 cm in diameter and can be one to two meters in length. This crystal is then sawed (like a loaf of bread) to produce circular wafers that are 400 μm to 600 μm thick (a micrometer, or micron, μm, is a millionth of a meter). The surface of the wafer is then polished to a mirror finish using chemical and mechanical polishing (CMP) techniques. Semiconductor manufacturers usually purchase ready-made silicon wafers from a supplier and rarely start their fabrication process in ingot form. The basic electrical and mechanical properties of the wafer depend on the orientation of the crystalline structure, the impurity concentrations, and the type of impurities present.

These variables are strictly controlled during crystal growth. A specific amount of impurities can be added to the pure silicon in a process known as doping. This allows the alteration of the electrical properties of the silicon, in particular its resistivity. Depending on the types of impurity, either holes (in *p*-type silicon) or electrons (in *n*-type silicon) can be responsible for electrical conduction. If a large number of impurity atoms is added, the silicon will be heavily doped (e.g., concentration > ~1018 atoms/cm-3). When designating the relative doping concentrations in semiconductor material, it is common to use the + and – symbols. A heavily doped (low-resistivity) *n*-type silicon wafer is referred to as *m*aterial, while a lightly doped material (e.g., concentration < ~1016 atoms/cm-3) is referred to as *n*-. Similarly, *p*+ and *p*- designations refer to the heavily doped and lightly doped *p*-type regions, respectively.

The ability to control the type of impurities and the doping concentration in the silicon permits the formation of diodes, transistors, and resistors in integrated circuits.

### A.1.2 Oxidation

In oxidation, silicon reacts with oxygen to form silicon dioxide (SiO2). To speed up this chemical reaction, it is necessary to carry out the oxidation at high temperatures quantities of contaminants (which could significantly alter the electrical properties of the C) and inside ultraclean furnaces. To avoid the introduction of even small

silicon), it is necessary to operate in a clean room . Particle filters are used to ensure that the airflow in the processing area is free from dust. All personnel must protect the clean-room environment by wearing special lint-free clothing that covers a person from head to toe.

The oxygen used in the reaction can be introduced either as a high-purity gas (referred to as a “dry oxidation”) or as steam (forming a “wet oxidation”). In general, wet oxidation has a faster growth rate, but dry oxidation gives better electrical characteristics. The thermally grown oxide layer has excellent electrical insulation properties. The dielectric strength for SiO2 is approximately 107 V/cm. It has a dielectric constant of about 3.9, and it can be used to form excellent MOS capacitors. Silicon dioxide can also serve as an effective mask against many impurities, allowing the introduction of dopants into the silicon only in regions that are not covered with oxide.

Silicon dioxide is a transparent film, and the silicon surface is highly reflective. If white light is shone on an oxidized wafer, constructive and destructive interference will cause certain colors to be reflected. The wavelengths of the reflected light depend on the thickness of the oxide layer. In fact, by categorizing the color of the wafer surface, one can deduce the thickness of the oxide layer. The same principle is used by more sophisticated optical infer meters to measure film thickness. On a processed wafer, there will be regions with different oxide thicknesses. The colors can be quite vivid and are immediately obvious when a finished wafer is viewed with the naked eye.

### A.1.3 Photolithography

Mass production with economy of scale is the primary reason for the tremendous impact VLSI has had on our society. The surface patterns of the various integrated-circuit components can be defined repeatedly using photolithography. The sequence of photolithographic steps is as illustrated in Fig. A.1.

The wafer surface is coated with a photosensitive layer called photoresist, using a spin- on technique. After this, a photographic plate with drawn patterns (e.g., a quartz plate with chromium layer for patterning) will be used to selectively expose the photoresist under a deep ultraviolet illumination (UV). The exposed areas will become softened (for positive photoresist). The exposed layer can then be removed using a chemical developer, causing

the mask pattern to be duplicated on the wafer. Very fine surface geometries can be reproduced accurately by this technique. Furthermore, the patterns can be projected directly onto the wafer, or by using a separate photo mask produced by a 10x "step and repeat" reduction technique as shown in Fig. A.2.

The patterned photoresist layer can be used as an effective masking layer to protect materials below from wet chemical etching or reactive ion etching (RIE). Silicon dioxide, silicon nitride, polysilicon, and metal layers can be selectively removed using the appropriate etching methods (see next section). After the etching step(s), the photoresist is stripped away, leaving behind a permanent pattern of the photo mask on the wafer surface. To make this process even more challenging, multiple masking layers (which can number more than 20 in advanced VLSI fabrication processes) must be aligned precisely on top of previous layers. This must be done with even finer precision than the minimum geometry size of the masking patterns. This requirement imposes very critical mechanical and optical constraints on the photolithography equipment.



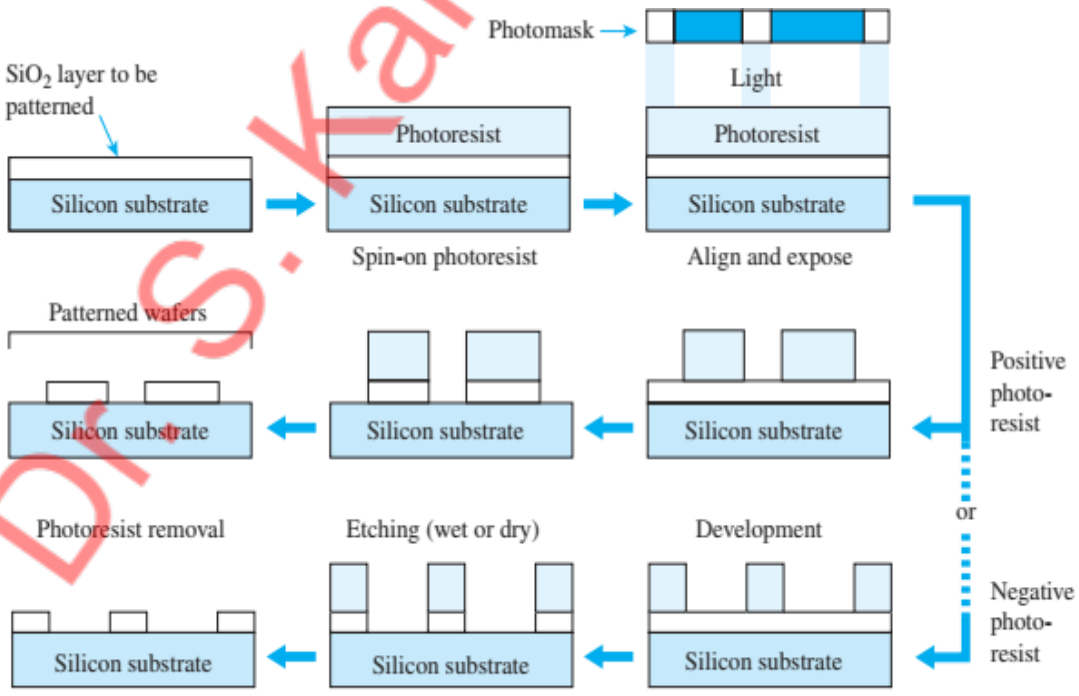



**Figure A.1** Photolithography using positive or negative photoresist.

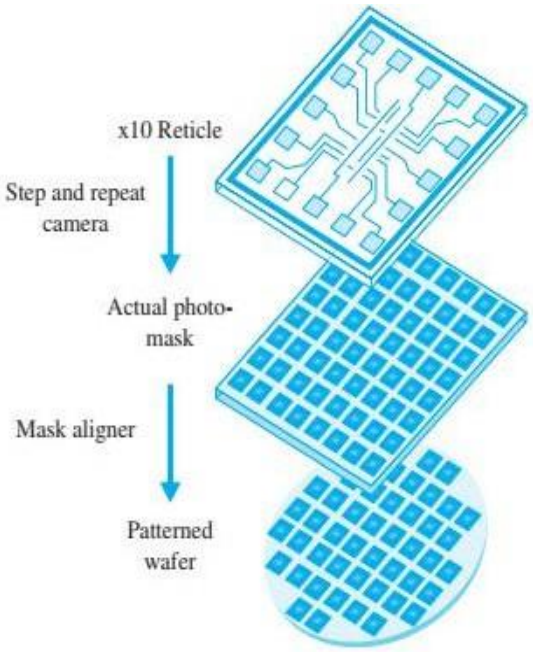



**Figure A.2** Conceptual illustration of a step-and-repeat reduction technique to facilitate the mass production of integrated circuits.



## Etching

To permanently imprint the photographic patterns onto the wafer, chemical (wet) etching or RIE dry etching procedures can be used. Chemical etching is usually referred to as wet etching. Different chemical solutions can be used to remove different layers. For example, hydrofluoric (HF) acid can be used to etch SiO2, potassium hydroxide (KOH) for silicon, phosphoric acid for aluminum, and so on. In wet etching, the chemical usually attacks the exposed regions that are not protected by the photoresist layer in all directions (isotropic etching). Depending on the thickness of the layer to be etched, a certain amount of undercut will occur. Therefore, the dimension of the actual pattern will differ slightly from the original pattern. If exact dimension is critical, RIE dry etching can be used. This method is essentially a directional bombardment of the exposed surface using a corrosive gas (or ions). The cross section of the etched layer is usually highly directional (anisotropic etching) and has the same dimension as the photoresist pattern. A comparison between isotropic and anisotropic etching is given in Fig. A.3.

## Diffusion

Diffusion is a process by which atoms move from a high-concentration region to a

low concentration region. This is very much like a drop of ink dispersing through a glass of water except that it occurs much more slowly in solids. In VLSI fabrication, this is a method to introduce impurity atoms (dopants) into silicon to change its resistivity. The rate at which dopants diffuse in silicon is a strong function of temperature. Diffusion of impurities is usually carried out at high temperatures desired doping profile. When the wafer is cooled to room temperature, the impurities are essentially "frozen" in position.

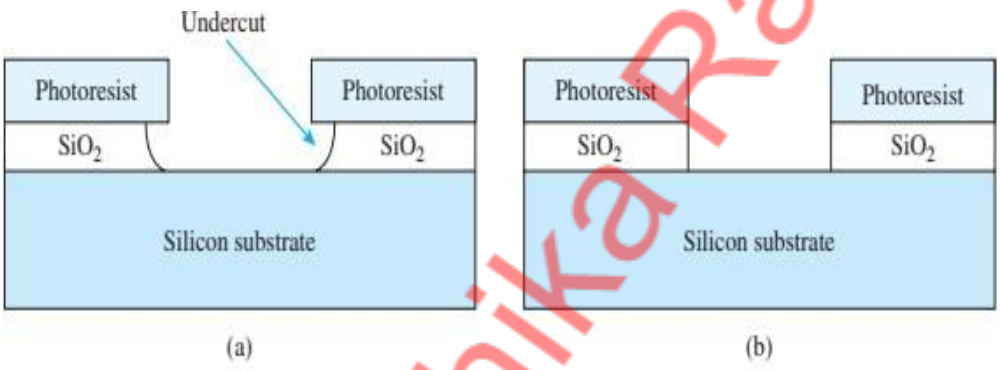



**Figure A.3** (**a**) Cross-sectional view of an isotropic oxide etch with severe undercut beneath the photoresist layer. (**b**) Anisotropic etching, which usually produces a cross section with no undercut.

The diffusion process is performed in furnaces similar to those used for oxidation. The depth to which the impurities diffuse depends on both the temperature and the processing time. The most common impurities used as dopants are boron, phosphorus, and arsenic. Boron is a *p*-type dopant, while phosphorus and arsenic are *n*-type dopants. These dopants can be effectively masked by thin silicon dioxide layers. By diffusing boron into an *n*-type substrate, a *pn* junction is formed (diode). If the doping concentration is heavy, the diffused layer can also be used as a conducting layer with very low resistivity.

**Ion Implantation**

Ion implantation is another method used to introduce impurities into the semiconductor crystal. An ion implanter produces ions of the desired dopant, accelerates them by an electric field, and allows them to strike the semiconductor surface. The ions become embedded in the crystal lattice. The depth of penetration is related to the energy of the ion beam, which can be controlled by the accelerating-field voltage. The quantity of ions

implanted can be controlled by varying the beam current (flow of ions). Since both voltage and current can be accurately measured and controlled, ion implantation results in impurity profiles that are much more accurate and reproducible than can be obtained by diffusion. In addition, ion implantation can be performed at room temperature. Ion implantation normally is used when accurate control of the doping profile is essential for device operation.

**Chemical Vapor Deposition**

Chemical vapor deposition (CVD) is a process by which gases or vapors are chemically reacted, leading to the formation of solids on a substrate. CVD can be used to deposit various materials on a silicon substrate including SiO2, Si3N4, polysilicon, and so on. For instance, if silane gas and oxygen are allowed to react above a silicon substrate, the end product, silicon dioxide, will be deposited as a solid film on the silicon wafer surface.

The properties of the CVD oxide layer are not as good as those of a thermally grown oxide, but they are sufficient to allow the layer to act as an electrical insulator. The advantage of a CVD layer is that the oxide deposits at a faster rate and a lower temperature (below 500°C). If silane gas alone is used, then a silicon layer will be deposited on the wafer. If the reaction temperature is high enough (above 1000°C), the layer deposited will be a crystalline layer (assuming that there is an exposed crystalline silicon substrate). Such a layer is called an epitaxial layer, and the deposition process is referred to as epitaxy instead of CVD.

At lower temperatures, or if the substrate surface is not single-crystal silicon, the atoms will not be able to aligned along the same crystalline direction. Such a layer is called polycrystalline silicon (poly Si), since it consists of many small crystals of silicon aligned in random fashion. Poly silicon layers are normally doped very heavily to form highly conductive regions that can be used for electrical interconnections.

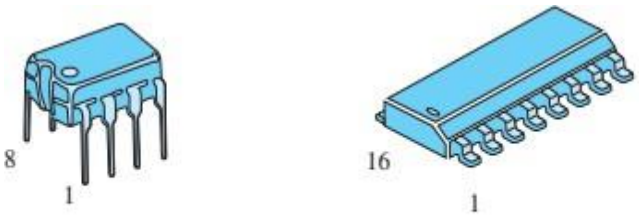



**Figure A.4** Examples of an 8-pin plastic dual-in-line IC package and a 16-pin surface-mount package.

The purpose of metallization is to interconnect the various components (transistors, capacitors, etc.) to form the desired integrated circuit. Metallization involves the deposition of a metal over the entire surface of the silicon. The required interconnection pattern is then selectively etched. The metal layer is normally deposited via a sputtering process. A pure metal disk (e.g., 99.99% aluminum target) is placed under an Ar (argon) ion gun inside a vacuum chamber.

The wafers are also mounted inside the chamber above the target. The Ar ions will not react with the metal, since argon is a noble gas. However, the ions are made to physically bombard the target and literally knock metal atoms out of the target. These metal atoms will then coat all the surface inside the chamber, including the wafers. The thickness of the metal film can be controlled by the length of the sputtering time, which is normally in the range of 1 to 2 minutes. The metal interconnects can then be defined using photolithography and etching steps.

**Packaging**

A finished silicon wafer may contain several hundreds of finished circuits or chips. A chip may contain from 10 to more than 108 transistors; each chip is rectangular and can be up to tens of millimeters on a side. The circuits are first tested electrically (while still in wafer form) using an automatic probing station. Bad circuits are marked for later identification. The circuits are then separated from each other (by dicing), and the good circuits (dies) are mounted in packages (headers). Examples of such IC packages are given in Fig. A.4. Fine gold wires are normally used to interconnect the pins of the package to the metallization pattern on the die. Finally, the package is sealed using plastic or epoxy under vacuum or in an inert atmosphere.

## Integrated Devices

Besides the obvious *n*- and *p*-channel MOSFETs, other devices can be obtained by appropriate masking patterns. These include *pn* junction diodes, MOS capacitors, and resistors.

## MOSFETs

The *n*-channel MOSFET is the preferred device in comparison to the *p*-MOSFET (Fig. A.6). The electron surface mobility is two to three times higher than that for holes. Therefore, with the same device size (*W* and *L*), the *n*-MOSFET offers higher current drive (or lower onresistance) and higher transconductance.

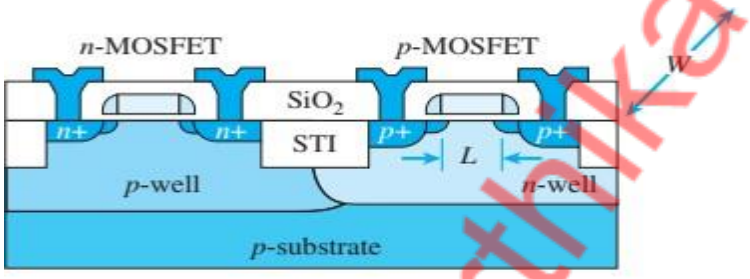



**Figure A.6** Cross-sectional diagram of *n*- and *p*-MOSFETs.

In an integrated-circuit design environment, MOSFETs are characterized by their threshold voltage and by their device sizes. Usually the *n*- and *p*-channel MOSFETs are designed to have threshold voltages of similar magnitude for a particular process. The transconductance can be adjusted by changing the device surface dimensions (*W* and *L*). This feature is not available for bipolar transistor, making the design of integrated MOSFET circuits much more flexible.

## Resistors

Resistors in integrated form are not very precise. They can be made from various diffusion regions as shown in Fig. A.7. Different diffusion regions have different resistivity. The *n* well is usually used for medium-value resistors, while the *n*+ and *p*+ diffusions are useful for low-value resistors. The actual resistance value can be defined by changing the length and width of diffused regions. The tolerance of the resistor value is

very poor (20–50%), but the matching of two similar resistor values is quite good (5%). Thus circuit designers should design circuits that exploit resistor matching and should avoid designs that require a specific resistor value.

All diffused resistors are self-isolated by the reverse-biased *pn* junctions. A serious drawback for these resistors is the fact that they are accompanied by a substantial parasitic junction capacitance, making them not very useful for high-frequency applications. The reverse-biased *pn* junctions also exhibit a JFET effect, leading to a variation in the resistance value as the supply voltage is changed (a large voltage coefficient is undesirable). Since the mobilities of carriers vary with temperature, diffused resistors also exhibit a significant temperature coefficient.

A more useful resistor can be fabricated using the polysilicon layer that is placed on top of the thick field oxide. The thin polysilicon layer provides better surface area matching and hence more accurate resistor ratios. Furthermore, the polyresistor is physically separated from the substrate, resulting in a much lower parasitic capacitance and voltage coefficient.

**Capacitors**

Two types of capacitor structure are available in CMOS processes: MOS and interpoly capacitors. The latter are also similar to metal–insulator–metal (MIM) capacitors. The cross sections of these structures are as shown in Fig. A.8. The MOS gate capacitance, depicted by the center structure, is basically the gate-to-source capacitance of a MOSFET. The capacitance value is dependent on the gate area. The oxide thickness is the same as the gate oxide thickness in the MOSFETs. This capacitor exhibits a large voltage dependence. To eliminate this problem, an addition $n+$ implant is required to form the bottom plate of the capacitors, as shown in the structure on the right. Both these MOS capacitors are physically in contact with the substrate, resulting in a large parasitic *pn* junction capacitance at the bottom plate.

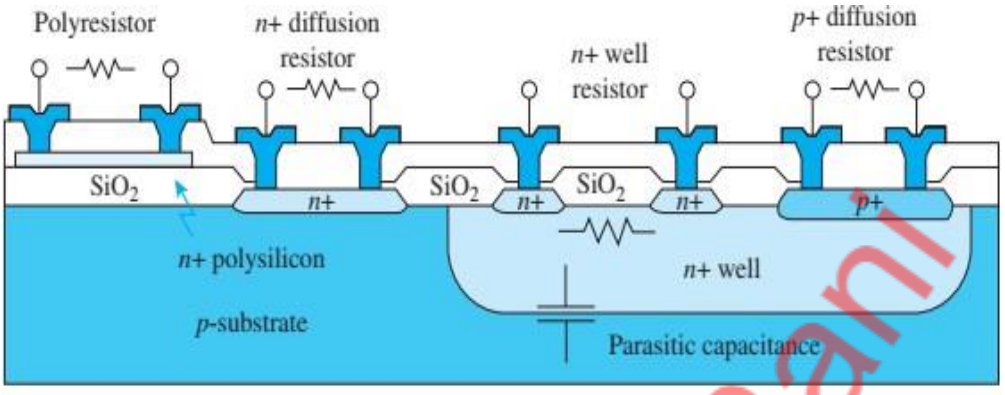



**Figure A.7** Cross sections of various resistor types available from a typical *n*-well CMOS process.

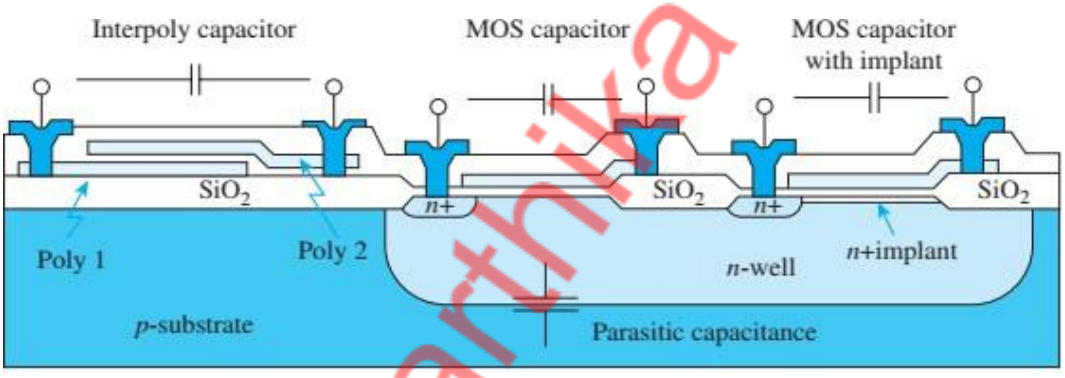



**Figure A.8** Interpoly and MOS capacitors in an *n*-well CMOS process.

The interpoly capacitor exhibits near-ideal characteristics but at the expense of the inclusion of a second polysilicon layer to the CMOS process. Since this capacitor is placed on top of the thick field oxide, parasitic effects are kept to a minimum.

A third and less often used capacitor is the junction capacitor. Any *pn* junction under reversed bias produces a depletion region that acts as a dielectric between the *p* and the *n* regions. The capacitance is determined by geometry and doping levels and has a large voltage coefficient. This type of capacitor is often used as a variactor (variable capacitor) for tuning circuits. However, this capacitor works only with reverse-bias voltages.

For the interpoly and MOS capacitors, the capacitance values can be controlled to within 1%. Practical capacitance values range from 0.5 pF to a few tens of picofarads. The

matching between capacitors of similar size can be within 0.1%. This property is extremely useful for designing precision analog CMOS circuits.

**PN Junction Diodes**

*n*-type and *p*-type diffusion regions are placed next to each other, a *pn* junction diode results. A useful structure is the *n*-well diode shown in Fig. A.9. The diode fabricated in an *n* well can provide a high breakdown voltage. This diode is essential for the input clamping circuits for protection against electrostatic discharge. The diode is also very useful as an on-chip temperature sensor by monitoring the variation of its forward voltage drop.

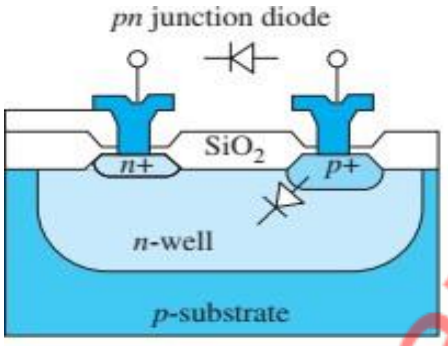



**Figure A.9** A *pn* junction diode in an *n*-well CMOS process.

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